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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/816,776
Filing Date: April 02, 2004
Appellant(s): JAIN ET AL.

Jay M. Cantor
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/13/06 appealing from the Office action mailed 3/28/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 7-9, 11-13, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mayur (US2003/0040130A1).

Mayur teaches all of the positive steps of claims 1-3, 5, 7-9, 11-13, and 15-18 except for explicitly teaching a temperature range of 1050-1350 degrees C..

Regarding claim 1, Mayur teaches providing a semiconductor (paragraph 0042), implanting a dopant species into the semiconductor (paragraph 0054) and annealing the implanted semiconductor at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1027 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, (Table II 1423 K (1150 C).

As paragraph 0054 teaches a temperature above 1027 degrees C., and limits melting to only surface melting (occurs at 1150 C), it is obvious that Mayur has anticipated a temperature of at least 23 more degrees and therefore teaches 1050 degrees C. Further, paragraph 0099 and Table II suggest that the temperature would not be above 1150 to avoid more than surface melting. Thus Mayur is suggesting a range of about 1027-1150 degrees C., within the range of the instant claims.

These ranges are considered to involve routine optimization while it has been held to be within the level of ordinary skill in the art. As noted in In re Aller (105 USPQ233), the selection of reaction parameters such as temperature and concentration would have been obvious:

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art. Such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
> In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

One skilled in the requisite art at the time of the invention would have used any ranges or exact figures suitable to the method in the process of annealing regarding time and temperature using prior knowledge, experimentation, and observation with the

apparatus used in order to optimize the process and produce the annealed structure desired to the parameters desired.

Regarding the duration of the annealing, Mayur teaches the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, recrystallization and dopant activation is complete in less than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

Regarding claim 2, the implant is amorphizing (paragraph 0054).

Regarding claim 3, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 5, Mayur teaches providing a semiconductor (paragraph 0042), a patterned photoresist layer (paragraph 0051), implanting a dopant species into semiconductor (paragraph 0054), removing the photoresist (figure 2C shows patterned photoresist removed), and annealing with a solid phase epitaxy anneal (paragraph 0043, epitaxial, paragraph 0084, solid phase and paragraph 0047, conventional anneal). Although Mayur does not recite "solid phase epitaxy anneal, this is inferred from the process (same as the instant application) and that it is a solid phase anneal resulting in an epitaxial layer.) The anneal is at an ultra high temperature of 1050-1350

degrees C. (paragraph 0007, greater than 1300K (1027 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

As paragraph 0054 teaches a temperature above 1027 degrees C., it is obvious that Mayur has anticipated a temperature of at least 24 more degrees and therefore teaches 1050 degrees C. Further, paragraph 0099 and Table II suggest that the temperature would not be above 1150 to avoid more than surface temperature. Thus Mayur is suggesting a range of about 1027-1150 degrees C., within the range of the instant claims.

Regarding the duration of the annealing, Mayur teaches the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, recrystallization and dopant activation is complete in less than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

These ranges are considered to involve routine optimization as recited above in regard to claim 1.

Regarding claim 7, the implant is amorphizing (paragraph 0054).

Regarding claim 8, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 9, Mayur teaches providing a semiconductor substrate (paragraph 0042), a gate dielectric layer (insulator 208), a gate electrode (210) on the gate dielectric, implanting dopant species into the semiconductor adjacent the gate electrodes (paragraph 0053), annealing the implanted semiconductor with solid phase epitaxy anneal between 550 and 950 C (paragraph 0047, diffusing dopants between 800-1100 C), and annealing at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1027 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

As paragraph 0054 teaches a temperature above 1027 degrees C., it is obvious that Mayur has anticipated a temperature of at least 24 more degrees and therefore teaches 1050 degrees C. Further, paragraph 0099 and Table II suggest that the temperature would not be above 1150 to avoid more than surface temperature. Thus Mayur is suggesting a range of about 1027-1150 degrees C., within the range of the instant claims.

Regarding the duration of the annealing, Mayur teaches the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, recrystallization and dopant activation is complete in less

than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

These ranges are considered to involve routine optimization as recited above in regard to claim 1.

Regarding claim 11, the amorphizing implant is preformed prior to the dopant implant (paragraph 0054).

Regarding claim 12, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 13, Mayur teaches forming a MOSFET transistor (paragraph 0006), providing a semiconductor substrate (paragraph 0042), a gate dielectric layer (insulator 208), a gate electrode (210) on the gate dielectric, implanting dopant species into the semiconductor adjacent the gate electrodes (paragraph 0053), implanting with gate sidewalls (as shown in figure 2F), annealing the implanted semiconductor with solid phase epitaxy anneal between 550 and 950 C (paragraph 0047, diffusing dopants between 800-1100 C), and annealing at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1027 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

As paragraph 0054 teaches a temperature above 1027 degrees C., it is obvious that Mayur has anticipated a temperature of at least 24 more degrees and therefore teaches 1050 degrees C. Further, paragraph 0099 and Table II suggest that the temperature would not be above 1150 to avoid more than surface temperature. Thus Mayur is suggesting a range of about 1027-1150 degrees C., within the range of the instant claims.

Regarding the duration of the annealing, Mayur teaches the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, recrystallization and dopant activation is complete in less than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

These ranges are considered to involve routine optimization as recited above in regard to claim 1.

Regarding claim 15, the amorphizing implant is preformed prior to the first dopant implant (paragraph 0054).

Regarding claims 16 and 17, the amorphizing implant (amorphous implant) is preformed prior to the second dopant implant (paragraph 0054, amorphizing implant performed prior to well implant and source/drain implant, two different species).

Regarding claim 18, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

(10) Response to Argument

the appellant argues that the claims limit the annealing temperature to between 1050 and 1350 degrees C and from about 0.5 to 3 milliseconds and that Mayur teaches a temperature of greater than 1027 degrees C (1300 K) for less than 50 milliseconds, and that the difference is so vast, that Mayur could not contemplate the instant invention.

Regarding the temperature, Mayur teaches a temperature above 1027 degrees C, and suggests that temperatures above 1150 would have deleterious results (melting). Thus a range of 1027-1150 is suggested. A temperature of above 1027 degrees would suggest to one of ordinary skill in the art a temperature of 1050 degrees, only 23 degrees higher. This is optimization as recited above in the rejection. By teaching that only surface melting is allowed, and by stating that this surface melting begins at 1150 degrees C (1423 K), Mayur is clearly suggesting an upper temperature limit of around 1150. the suggested range of Mayur (1027-1150) encompasses 100 degrees of the 300-degree range of the instant claims. As stated above, Mayur suggests a range within the range of the instant claim.

Regarding the time duration of the anneal, Mayur teaches a time less than 50 milliseconds, and that reads on the claims. Further, Mayur dopant activation is complete

in less than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the entire claimed range.

Even if Mayur did not contemplate the instant invention, one of ordinary skill in the requisite art upon reading Mayur, would achieve the results of the instant invention by practicing Mayur, within the suggested or optimized ranges of time and temperature.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

David S. Blum

Conferees:

Carl Whitehead Jr. Ricky Mack